Phison Electronics Corporation

PS5007-E7 2.5” PCIe SSD Specification

Version 1.5

Phison Electronics Corporation

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Revision History

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0.2	2015/01/27	Performance update	Larry Li
0.3	2015/02/06	Add minimum average P/E cycles information	Justina Lai
0.4	2015/04/30	Modify Environmental Conditions	Larry Li
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1.4	2016/07/27	Update performance and TBW formula	Larry Li
1.5	2016/08/24	1.Add 2pln flash performance and TBW 2.Add pSLC performance and TBW	Justina Lai

Product Overview

- **Capacity**
  - MLC: 240GB up to 1,920GB (256GB up to 2TB)
  - pSLC: 120GB up to 960GB (128GB up to 1,024GB)
- **Form Factor**
  - U.2
- **PCIe Interface**
  - PCIe Gen3 x 4
- **Compliance**
  - NVMe 1.2
  - PCI Express Base 3.0
- **Flash Interface**
  - Flash Type: MLC
  - 2pcs to 16pcs of BGA flash
- **Performance**
  - Read: up to 2,800 MB/s
  - Write: up to 1,550 MB/s
- **Power Consumption**[Note1]
  - Active mode: < 7.3W
- **TBW (Terabytes Written)** [Note2]
  - MLC: 2,793 TBW
  - pSLC: 16,756 TBW
- **MTBF**
  - More than 2,000,000 hours
- **Advanced Flash Management**
  - Static and Dynamic Wear Leveling
  - Bad Block Management
  - TRIM
  - SMART
  - Over-Provision
  - Firmware Update
- **Power Saving Mode**
  - Support APST
  - Support ASPM
  - Support L1.2
- **Temperature Range**
  - Operation: 0°C ~ 70°C
  - Storage: -40°C ~ 85°C
- **RoHS compliant**

Notes:

1. Please see “4.2 Power Consumption” for details.
2. Please see “TBW (Terabytes Written)” in Chapter 2” for details.

Performance and Power Consumption

Capacity	Flash Structure	Performance				Power Consumption		
		CrystalDiskMark		ATTO		Read (mW)	Write (mW)	Idle (mW)
		Read (MB/s)	Write (MB/s)	Read (MB/s)	Write (MB/s)			
240GB (256GB)	32GB x 8, BGA, 15nm MLC (4pln)	2,750	1,500	3,000	2,200	2,940	4,690	500
480GB (512GB)	64GB x 8, BGA, 15nm MLC (4pln)	2,800	1,550	3,000	2,200	5,570	7,270	500
960GB (1TB)	128GB x 8, BGA, 15nm MLC (4pln)	2,800	1,550	3,000	2,200	5,580	7,275	500
1,920GB (2TB)	256GB x 16, BGA, 15nm MLC (4pln)	2,800	1,550	3,000	2,200	5,580	7,200	500
240GB (256GB)	32GB x 8, BGA, 15nm MLC (2pln)	2,750	1,350	3,000	2,200	2,940	4,690	500
480GB (512GB)	64GB x 8, BGA, 15nm MLC (2pln)	2,800	1,500	3,000	2,200	5,570	7,270	500
960GB (1TB)	128GB x 8, BGA, 15nm MLC (2pln)	2,800	1,500	3,000	2,200	5,580	7,275	500
1,920GB (2TB)	256GB x 16, BGA, 15nm MLC (2pln)	2,800	1,500	3,000	2,200	5,580	7,200	500
120GB (128GB)	32GB x 8, BGA, 15nm pSLC (4pln)	2,750	1,500	3,000	2,200	2,940	4,690	500
240GB (256GB)	64GB x 8, BGA, 15nm pSLC (4pln)	2,800	1,550	3,000	2,200	5,570	7,270	500
480GB (512GB)	128GB x 8, BGA, 15nm pSLC (4pln)	2,800	1,550	3,000	2,200	5,580	7,275	500
960GB (1TB)	256GB x 16, BGA, 15nm pSLC (4pln)	2,800	1,550	3,000	2,200	5,580	7,200	500

NOTE:

(1) For more details on Power Consumption, please refer to Chapter 4.2.

(2) The performance above is based on 15nm MLC to estimate.

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1. INTRODUCTION

1.1. General Description

Phison 2.5” PCIe SSD delivers all the advantages of flash disk technology with PCIe Gen3 x4 interface, including being compliant with standard 2.5-inch form factor and SFF-8639 connector, providing low power consumption compared to traditional hard drive and hot-swapping when removing/replacing/upgrading flash disks. The device is designed based on the standard 38-pin interface for data segment and 15-pin for power segment, as well as operating at a maximum operating frequency of 200MHz with 25MHz external crystal. Its capacity could provide a wide range up to 1,920GB. Moreover, it can reach up to 2,800MB/s read as well as 1,550MB/s write high performance based on Toshiba’s 15nm Toggle MLC flash (with 256MB/512MB/1024MB/2048 DDR3 cache enabled and measured by CrystalDiskMark v5.0). Meanwhile, the power consumption of the 2.5” PCIe SSD is much lower than traditional hard drives.

1.2. Controller Block Diagram

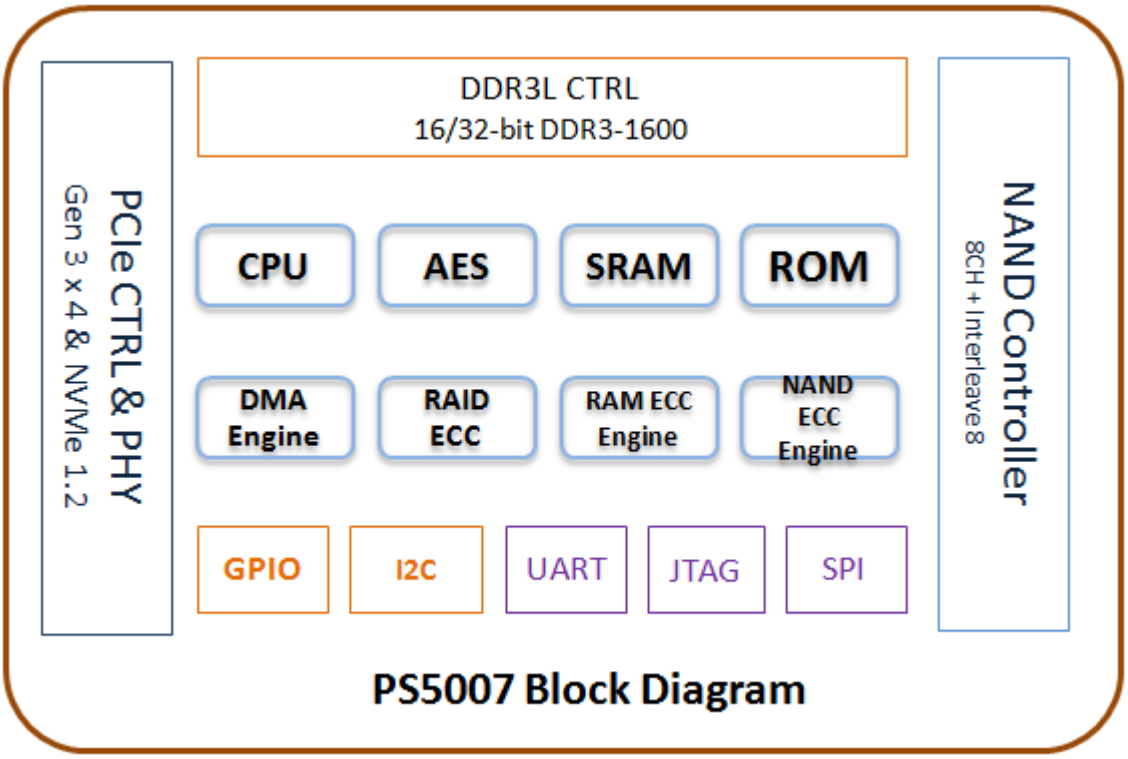


Figure 1-1 PS5007-E7 2.5’’ PCIe SSD Controller Block Diagram

1.3. Product Block Diagram

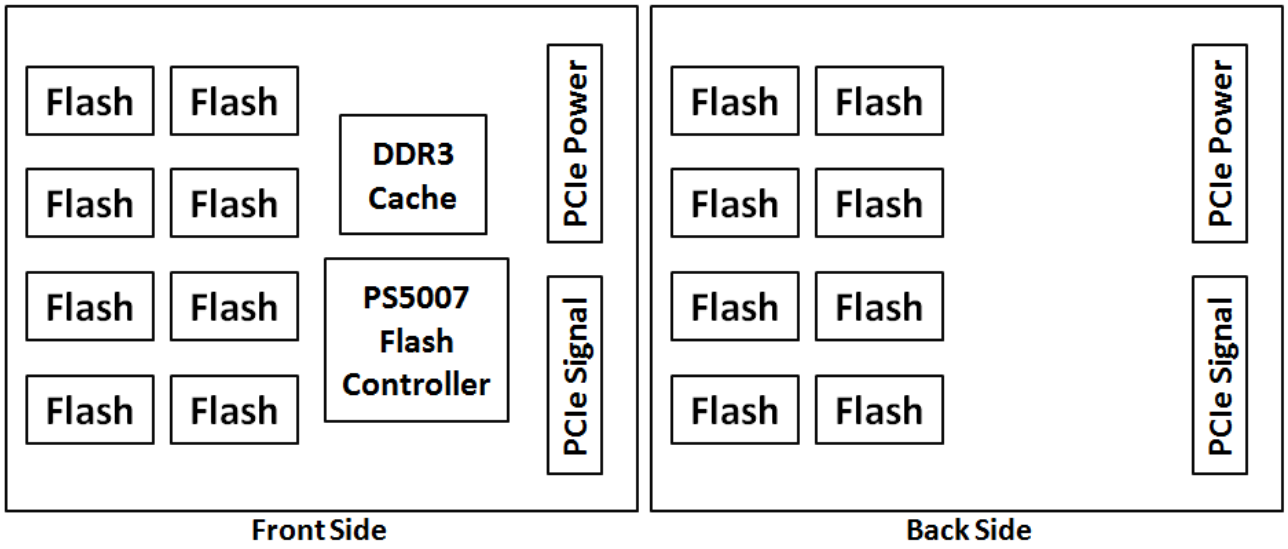


Figure 1-2 PS5007-E7 2.5'' PCIe SSD Product Block Diagram

1.4. Flash Management

1.4.1. Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, PS5007-E7 PCIe SSD applies the BCH ECC algorithm, which can detect and correct errors occur during read process, ensure data been read correctly, as well as protect data from corruption.

1.4.2. Wear Leveling

NAND flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some areas get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.

Phison provides advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND flash is greatly improved.

1.4.3. Bad Block Management

Bad blocks are blocks that include one or more invalid bits, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Initial Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. Phison implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages any bad blocks that appear with use. This practice further prevents data being stored into bad blocks and improves the data reliability.

1.4.4. TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid-state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD which blocks of data are no longer in use and can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks all the time.

1.4.5. SMART

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a hard disk drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users of impending failures while there is still time to perform proactive actions, such as copy data to another device.

1.4.6. Over-Provision

Over Provisioning refers to the inclusion of extra NAND capacity in a SSD, which is not visible and cannot be used by users. With Over Provisioning, the performance and IOPS (Input/Output Operations per Second) are improved by providing the controller additional space to manage P/E cycles, which enhances the reliability and endurance as well. Moreover, the write amplification of the SSD becomes lower when the controller writes data to the flash.

1.4.7. Firmware Upgrade

Firmware can be considered as a set of instructions on how the device communicates with the host. Firmware will be upgraded when new features are added, compatibility issues are fixed, or read/write performance gets improved.

1.5. Power Loss Protection: Flushing Mechanism

Power Loss Protection is a mechanism to prevent data loss during unexpected power failure. DRAM is a volatile memory and frequently used as temporary cache or buffer between the controller and the NAND flash to improve the SSD performance. However, one major concern of the DRAM is that it is not able to keep data during power failure. Accordingly, the PS5007-E7 applies the ***GuaranteedFlush*** technology, which requests the controller to transfer data to the cache. For PS5007-E7, DDR performs as a cache, and its sizes include 256MB, 512MB, 1024MB or 2048MB. Only when the data is fully committed to the NAND flash will the controller send acknowledgement (ACK) to the host. Such implementation can prevent false-positive performance and the risk of power cycling issues.

Additionally, it is critical for a controller to shorten the time the in-flight data stays in the cache. Thus, Phison's PS5007-E7 applies an algorithm to reduce the amount of data resides in the cache to provide a better performance. This ***SmartCacheFlush*** technology allows incoming data to only have a "pit stop" in the cache and then move to the NAND flash at once. If the flash is jammed due to particular file sizes (such as random 4KB data), the cache will be treated as an "organizer", consolidating incoming data into groups before written into the flash to improve write amplification.

In sum, with Flush Mechanism, PS5007-E7 proves to provide the reliability required by consumer, industrial, and enterprise-level applications.

1.6. Advanced Device Security Features

1.6.1. Secure Erase

Secure Erase is a standard NVMe format command and will write all "0xFF" to fully wipe all the data on hard drives and SSDs. When this command is issued, the SSD controller will empty its storage blocks and return to its factory default settings.

1.6.2. Write Protect

When a SSD contains too many bad blocks and data are continuously written in, then the SSD might not be usable anymore. Thus, Write Protect is a mechanism to prevent data from being written in and protect the accuracy of data that are already stored in the SSD.

1.7. SSD Lifetime Management

1.7.1. Terabytes Written (TBW)

TBW (Terabytes Written) is a measurement of SSDs' expected lifespan, which represents the amount of data written to the device. To calculate the TBW of a SSD, the following equation is applied:

TBW = [(NAND Endurance) x (SSD Capacity)] / [WAF]

NAND Endurance: NAND endurance refers to the P/E (Program/Erase) cycle of a NAND flash.

SSD Capacity: The SSD capacity is the specific capacity in total of a SSD.

WAF: Write Amplification Factor (WAF) is a numerical value representing the ratio between the amount of data that a SSD controller needs to write and the amount of data that the host's flash controller writes. A better WAF, which is near 1, guarantees better endurance and lower frequency of data written to flash memory.

1.8. An Adaptive Approach to Performance Tuning

1.8.1. Throughput

Based on the available space of the disk, PS5007-E7 will regulate the read/write speed and manage the performance of throughput. When there still remains a lot of space, the firmware will continuously perform read/write action. There is still no need to implement garbage collection to allocate and release memory, which will accelerate the read/write processing to improve the performance. Contrarily, when the space is going to be used up, PS5007-E7 will slow down the read/write processing, and implement garbage collection to release memory. Hence, read/write performance will become slower.

1.8.2. Predict & Fetch

Normally, when the Host tries to read data from the PCIe SSD, the PCIe SSD will only perform one read action after receiving one command. However, PS5007-E7 applies ***Predict & Fetch*** to improve the read speed. When the host issues sequential read commands to the PCIe SSD, the PCIe SSD will automatically expect that the following will also be read commands. Thus, before receiving the next command, flash has already prepared the data. Accordingly, this accelerates the data processing time, and the host does not need to wait so long to receive data.

2. PRODUCT SPECIFICATIONS

- **Capacity**
  - Supported capacity[Note1] : 240GB, 480GB, 960GB, 1,920GB, 256B, 512GB, 1TB, 2TB (support 48-bit addressing mode)
- **Electrical/Physical Interface**
  - PCIe Interface
    - Compliant with NVMe 1.2
    - Compatible with PCIe I/II/III x 4 interface
    - Support up to queue depth 64K
    - Support power management
- **Supported NAND Flash**
  - Toshiba 15nm MLC, pSLC Toggle 1.0 and Toggle 2.0
  - Support all types of MLC large block: 8KB/page and 16K/page page NAND flash
  - Contain 2pcs to 16pcs of BGA flash
- **ECC Scheme**
  - PS5007-E7 2.5” PCIe SSD can correct up to 120 bits error in 2K Byte data.
- **UART function**
- **GPIO**
- **Support SMART and TRIM commands**

- **Performance**

Capacity	Flash Structure	Flash Type	Sequential	
			Read (MB/s)	Write (MB/s)
240GB (256GB)	32GB x 8	BGA, 15nm MLC (4pln)	2,750	1,500
480GB (512GB)	64GB x 8	BGA, 15nm MLC (4pln)	2,800	1,550
960GB (1TB)	128GB x 8	BGA, 15nm MLC (4pln)	2,800	1,550
1,920GB (2TB)	128GB x 16	BGA, 15nm MLC (4pln)	2,800	1,550
240GB (256GB)	32GB x 8	BGA, 15nm MLC (2pln)	2,750	1,350
480GB (512GB)	64GB x 8	BGA, 15nm MLC (2pln)	2,800	1,500
960GB (1TB)	128GB x 8	BGA, 15nm MLC (2pln)	2,800	1,500
1,920GB (2TB)	128GB x 16	BGA, 15nm MLC (2pln)	2,800	1,500
120GB (128GB)	32GB x 8	BGA, 15nm pSLC (4pln)	2,750	1,500
240GB (256GB)	64GB x 8	BGA, 15nm pSLC (4pln)	2,800	1,550
480GB (512GB)	128GB x 8	BGA, 15nm pSLC (4pln)	2,800	1,550
960GB (1TB)	128GB x 16	BGA, 15nm pSLC (4pln)	2,800	1,550

NOTES:

1. The performance was estimated based on Toshiba 15nm MLC NAND flash.
2. Performance may differ according to flash configuration and platform.
3. The table above is for reference only. The criteria for MP (mass production) and for accepting goods shall be discussed based on different flash configuration.

● **TBW (Terabytes Written)**

Capacity	Flash Structure	TBW
240GB (256GB)	BGA, 15nm MLC (4pln)	349
480GB (512GB)	BGA, 15nm MLC (4pln)	698
960GB (1TB)	BGA, 15nm MLC (4pln)	1,396
1,920GB (2TB)	BGA, 15nm MLC (4pln)	2,793
240GB (256GB)	BGA, 15nm MLC (2pln)	349
480GB (512GB)	BGA, 15nm MLC (2pln)	698
960GB (1TB)	BGA, 15nm MLC (2pln)	1,396
1,920GB (2TB)	BGA, 15nm MLC (2pln)	2,793
120GB (128GB)	BGA, 15nm pSLC (4pln)	2,094
240GB (256GB)	BGA, 15nm pSLC (4pln)	4,189
480GB (512GB)	BGA, 15nm pSLC (4pln)	8,378
960GB (1TB)	BGA, 15nm pSLC (4pln)	16,756

NOTES:

1. Samples were built using Toshiba 15nm Toggle MLC NAND flash.
2. TBW may differ according to flash configuration and platform.
3. Follow JEDEC 219 pattern to test WAF.
4. The endurance of SSD could be estimated based on user behavior, NAND endurance cycles, and write amplification factor. It is not guaranteed by flash vendor.

3. ENVIRONMENTAL SPECIFICATIONS

3.1. Environmental Conditions

3.1.1. Temperature and Humidity

- Temperature:
  - Storage: -40°C to 85°C
  - Operational: 0°C to 70°C
- Humidity: RH 90% under 40°C (operational)

Table 3-1 High Temperature Test Condition

	Temperature	Humidity	Test Time
Operation	70°C	0% RH	72 hours
Storage	85°C	0% RH	72 hours

Result: No any abnormality is detected.

Table 3-2 Low Temperature Test Condition

	Temperature	Humidity	Test Time
Operation	0°C	0% RH	72 hours
Storage	-40°C	0% RH	72 hours

Result: No any abnormality is detected.

Table 3-3 High Humidity Test Condition

	Temperature	Humidity	Test Time
Operation	40°C	90% RH	4 hours
Storage	40°C	93% RH	72 hours

Result: No any abnormality is detected.

Table 3-4 Temperature Cycle Test

	Temperature	Test Time	Cycle
Operation	0°C	30 min	10 Cycles
	70°C	30 min	
Storage	-40°C	30 min	10 Cycles
	85°C	30 min	

Result: No any abnormality is detected.

3.1.2. Shock

Table 3-5 PS5007-E7 2.5'' PCIe SSD Shock Specification

	Acceleration Force	Half Sin Pulse Duration
Non-operational	1500G	0.5ms

Result: No any abnormality is detected when power on.

3.1.3. Vibration

Table 3-6 PS5007-E7 2.5'' PCIe SSD Vibration Specification

	Condition		Vibration Orientation
	Frequency/Displacement	Frequency/Acceleration	
Non-operational	20Hz~80Hz/1.52mm	80Hz~2000Hz/20G	X, Y, Z axis/30 min for each

Result: No any abnormality is detected when power on.

3.1.4. Drop

Table 3-7 PS5007-E7 2.5'' PCIe SSD Drop Specification

	Height of Drop	Number of Drop
Non-operational	80cm free fall	6 face of each unit

Result: No any abnormality is detected when power on.

3.1.5. Bending

Table 3-8 PS5007-E7 2.5'' PCIe SSD Bending Specification

	Force	Action
Non-operational	≥ 50N	Hold 1min/5times

Result: No any abnormality is detected when power on.

3.1.6. Torque

Table 3-9 PS5007-E7 2.5'' PCIe SSD Torque Specification

	Force	Action
Non-operational	1.263N-m or ±10 deg	Hold 1min/5times

Result: No any abnormality is detected when power on.

3.1.7. Electrostatic Discharge (ESD)

Table 3-10 PS5007-E7 2.5'' PCIe SSD Contact ESD Specification

Device	Capacity	Temperature	Relative Humidity	+/- 4KV	Result
2.5'' PCIe SSD	960GB/ 480GB	24.0°C	49% (RH)	Device functions are affected, but EUT will be back to its normal or operational state automatically.	PASS

3.1.8. EMI Compliance

- FCC: CISPR22
- CE: EN55022
- BSMI 13438

3.2. MTBF

MTBF, an acronym for Mean Time Between Failures, is a measure of a device's reliability. Its value represents the average time between a repair and the next failure. The measure is typically in units of hours. The higher the MTBF value, the higher the reliability of the device. The predicted result of Phison's PS5007-E7 2.5'' PCIe SSD is more than 2,000,000 hours.

3.3. Certification & Compliance

- RoHS
- PCI Express Base 3.0
- UNH-IOL NVM Express Logo

4. ELECTRICAL SPECIFICATIONS

4.1. Supply Voltage

Table 4-1 Supply Voltage of PS5007-E7 2.5'' PCIe SSD

Parameter	Rating
Operating Voltage	12V +/- 8%

4.2. Power Consumption

Table 4-2 Power Consumption of PS5007-E7 2.5'' PCIe SSD

Capacity	Flash Structure	Flash Type	Read	Write	Idle
240GB (256GB)	32GB x 8	BGA, 15nm(4pln)	2,940	4,690	500
480GB (512GB)	64GB x 8	BGA, 15nm(4pln)	5,570	7,270	500
960GB (1TB)	128GB x 8	BGA, 15nm(4pln)	5,580	7,275	500
1,920GB (2TB)	128GB x 16	BGA, 15nm(4pln)	5,580	7,200	500

Unit: mW

NOTES:

1. The average value of power consumption is achieved based on 100% conversion efficiency.
2. The measured power voltage is 12V.
3. Samples were built of Toshiba 15nm Toggle MLC NAND flash and measured under ambient temperature.
4. Sequential R/W is measured while testing 1MB sequential R/W 3 times by IOMeter.
5. Power Consumption may differ according to flash configuration and platform.

5. INTERFACE

5.1. Pin Assignment and Descriptions

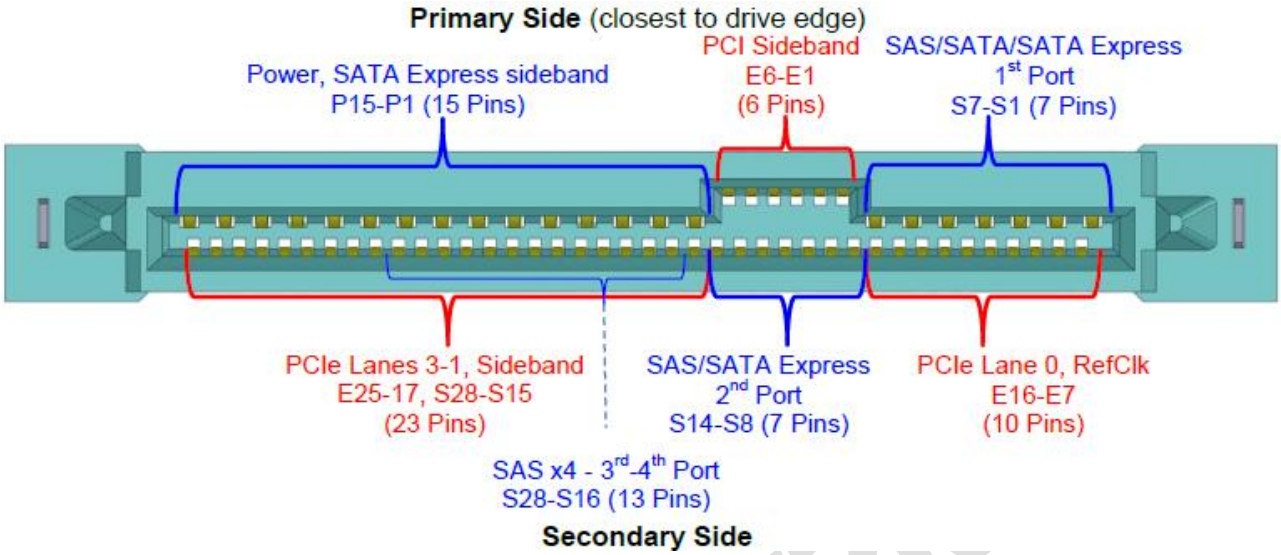


Figure 5-1 PS5007-E7 2.5'' PCIe SSD Pin Locations

Table 5-1 2.5" PCIe SSD SFF-8639 Connector Pin Assignment and Descriptions

Pin Number	Name	Type	Description
P1	WAKE#	Input	Signal for Link reactivation
P2	-	-	Outside scope of this specification
P3	CLKREQ#	Bi-Dir	Clock request
P4	IfDet#	Input	Interface Type Detect
P5	Ground	Ground	Ground
P6	Ground	Ground	Ground
P7	-	-	Outside scope of this specification
P8	-	-	Outside scope of this specification
P9	-	-	Outside scope of this specification
P10	PRSNT#	Input	Presence detect
P11	Activity	Input	
P12	Ground	Ground	Ground
P13	+12V Precharge	Power	+12V Precharge power for SFF-8639 module
P14	+12V	Power	+12V power for SFF-8639 module
P15	+12V	Power	+12V power for SFF-8639 module
S1	Ground	Ground	Ground
S2	-	-	Outside scope of this specification
S3	-	-	Outside scope of this specification
S4	Ground	Ground	Ground

Pin Number	Name	Type	Description
S5	-	-	Outside scope of this specification
S6	-	-	Outside scope of this specification
S7	Ground	Ground	Ground
S8	Ground	Ground	Ground
S9	-	-	Outside scope of this specification
S10	-	-	Outside scope of this specification
S11	Ground	Ground	Ground
S12	-	-	Outside scope of this specification
S13	-	-	Outside scope of this specification
S14	Ground	Ground	Ground
S15	Reserved	-	Reserved
S16	Ground	Ground	Ground
S17	PETp1	Diff-Pair	Transmitter differential pair, Lane 1
S18	PETn1	Diff-Pair	Transmitter differential pair, Lane 1
S19	Ground	Ground	Ground
S20	PERn1	Diff-Pair	Receiver differential pair, Lane 1
S21	PERp1	Diff-Pair	Receiver differential pair, Lane 1
S22	Ground	Ground	Ground
S23	PETp2	Diff-Pair	Transmitter differential pair, Lane 2
S24	PETn2	Diff-Pair	Transmitter differential pair, Lane 2
S25	Ground	Ground	Ground
S26	PERn2	Diff-Pair	Receiver differential pair, Lane 2
S27	PERp2	Diff-Pair	Receiver differential pair, Lane 2
S28	Ground	Ground	Ground
E1	REFCLKB+	Diff-Pair	Reference clock (differential pair) for second X2 port
E2	REFCLKB-	Diff-Pair	Reference clock (differential pair) for second X2 port
E3	+3.3 Vaux	Power	3.3 V auxiliary power
E4	PERSTB#	Output	Fundamental reset for second X2 port
E5	PERST#	Output	Fundamental reset (if dual-port enabled, first X2 port)
E6	Reserved	-	Reserved
E7	REFCLK+	Diff-Pair	Reference clock (if dual-port enabled, first X2 port)
E8	REFCLK-	Diff-Pair	Reference clock (if dual-port enabled, first X2 port)
E9	Ground	Ground	Ground
E10	PETp0	Diff-Pair	Transmitter differential pair, Lane 0
E11	PETn0	Diff-Pair	Transmitter differential pair, Lane 0
E12	Ground	Ground	Ground
E13	PERn0	Diff-Pair	Receiver differential pair, Lane 0
E14	PERp0	Diff-Pair	Receiver differential pair, Lane 0

Pin Number	Name	Type	Description
E15	Ground	Ground	Ground
E16	Reserved	-	Reserved
E17	PETp3	Diff-Pair	Transmitter differential pair, Lane 3
E18	PETn3	Diff-Pair	Transmitter differential pair, Lane 3
E19	Ground	Ground	Ground
E20	PERn3	Diff-Pair	Receiver differential pair, Lane 3
E21	PERp3	Diff-Pair	Receiver differential pair, Lane 3
E22	Ground	Ground	Ground
E23	SMCLK	Bi-Dir	SMBus (System Management Bus) clock
E24	SMDAT	Bi-Dir	SMBus (System Management Bus) data
E25	DualPortEn#	Output	Dual-port Enable

6. SUPPORTED COMMANDS

6.1. NVMe Command List

Table 6-1 Admin Commands

Opcode	Command Description
00h	Delete I/O Submission Queue
01h	Create I/O Submission Queue
02h	Get Log Page
04h	Delete I/O Completion Queue
05h	Create I/O Completion Queue
06h	Identify
08h	Abort
09h	Set Features
0Ah	Get Features
0Ch	Asynchronous Event Request
10h	Firmware Activate
11h	Firmware Image Download

Table 6-2 Admin Commands – NVM Command Set Specific

Opcode	Command Description
80h	Format NVM
81h	Security Send
82h	Security Receive

Table 6-3 NVM Commands

Opcode	Command Description
00h	Flush
01h	Write
02h	Read
04h	Write Uncorrectable
05h	Compare
08h	Write Zeroes
09h	Dataset Management

6.2. Identify Device Data

The following table details the sector data returned by the IDENTIFY DEVICE command.

Table 6-4 Identify Controller Data Structure

Bytes	O/M	Description	Default Value
01:00	M	PCI Vendor ID (VID)	0x1987
03:02	M	PCI Subsystem Vendor ID (SSVID)	0x1987
23:04	M	Serial Number (SN)	SN
63:24	M	Model Number (MN)	Model Number
71:64	M	Firmware Revision (FR)	FW Name
72	M	Recommended Arbitration Burst (RAB)	0x01
75:73	M	IEEE OUI Identifier (IEEE)	0
76	O	Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC)	0x00
77	M	Maximum Data Transfer Size (MDTS)	0x09
79:78	M	Controller ID (CNTLID)	0x0000
83:80	M	Version (VER)	0x00010200
87:84	M	RTD3 Resume Latency (RTD3R)	0x00124F80
91:88	M	RTD3 Entry Latency (RTD3E)	0x0016E360
95:92	M	Optional Asynchronous Events Supported (OAES)	0
239:96	-	Reserved	0
255:240	-	Refer to the NVMe Management Interface Specification for definition	0
257:256	M	Optional Admin Command Support (OACS)	0x0007
258	M	Abort Command Limit (ACL)	0x03
259	M	Asynchronous Event Request Limit (AERL)	0x03
260	M	Firmware Updates (FRMW)	0x02
261	M	Log Page Attributes (LPA)	0x03
262	M	Error Log Page Entries (ELPE)	0x3F
263	M	Number of Power States Support (NPSS)	0x04
264	M	Admin Vendor Specific Command Configuration (AVSCC)	0x01
265	O	Autonomous Power State Transition Attributes (APSTA)	0x01
267:266	M	Warning Composite Temperature Threshold (WCTEMP)	0x0157
269:268	M	Critical Composite Temperature Threshold (CCTEMP)	0x0193
271:270	O	Maximum Time for Firmware Activation (MTFA)	0x0000
275:272	O	Host Memory Buffer Preferred Size (HMPRE)	0
279:276	O	Host Memory Buffer Minimum Size (HMMIN)	0
295:280	O	Total NVM Capacity (TNVMCAP)	0
311:296	O	Unallocated NVM Capacity (UNVMCAP)	0

Bytes	O/M	Description	Default Value
315:312	O	Replay Protected Memory Block Support (RPMBS)	0
511:316	-	Reserved	0
NVM Command Set Attributes			
512	M	Submission Queue Entry Size (SQES)	0x66
513	M	Completion Queue Entry Size (CQES)	0x44
515:514	-	Reserved	0
519:516	M	Number of Namespaces (NN)	0x01
521:520	M	Optional NVM Command Support (ONCS)	0x001E
523:522	M	Fused Operation Support (FUSES)	0
524	M	Format NVM Attributes (FNA)	0
525	M	Volatile Write Cache (VWC)	0x01
527:526	M	Atomic Write Unit Normal (AWUN)	0x00FF
529:528	M	Atomic Write Unit Power Fail (AWUPF)	0x00
530	M	NVM Vendor Specific Command Configuration (NVSCC)	0x01
531	M	Reserved	0
533:532	O	Atomic Compare & Write Unit (ACWU)	0x00
535:534	M	Reserved	0
539:536	O	SGL Support (SGLS)	0x00
703:540	M	Reserved	0
IO Command Set Attributes			
2047:704	M	Reserved	0
2048:2079	M	Power State 0 Descriptor	PSD0
2111:2080	O	Power State 1 Descriptor	PSD1
2143:2112	O	Power State 2 Descriptor	PSD2
2175:2144	O	Power State 3 Descriptor	PSD3
2207:2176	O	Power State 4 Descriptor	PSD4
…	-	(N/A)	0
3071:3040	O	Power State 31 Descriptor	PSD31
Vendor Specific			
4095:3072	O	Vendor Specific (VS)	Phison Reserved

Table 6-5 Identify Namespace Data Structure & NVM Command Set Specific

Bytes	Description
7:0	Namespace Size (NSZE)
15:8	Namespace Capacity (NCAP)
23:16	Namespace Utilization (NUSE)
24	Namespace Features (NSFEAT)
25	Number of LBA Formats (NLBAF)
26	Formatted LBA Size (FLBAS)
27	Metadata Capabilities (MC)
28	End-to-end Data Protection Capabilities (DPC)
29	End-to-end Data Protection Type Settings (DPS)
30	Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC)
31	Reservation Capabilities (RESCAP)
119:32	Reserved
127:120	IEEE Extended Unique Identifier (EUI64)
131:128	LBA Format 0 Support (LBAF0)
135:132	LBA Format 1 Support (LBAF1)
139:136	LBA Format 2 Support (LBAF2)
143:140	LBA Format 3 Support (LBAF3)
147:144	LBA Format 4 Support (LBAF4)
151:148	LBA Format 5 Support (LBAF5)
155:152	LBA Format 6 Support (LBAF6)
159:156	LBA Format 7 Support (LBAF7)
163:160	LBA Format 8 Support (LBAF8)
167:164	LBA Format 9 Support (LBAF9)
171:168	LBA Format 10 Support (LBAF10)
175:172	LBA Format 11 Support (LBAF11)
179:176	LBA Format 12 Support (LBAF12)
183:180	LBA Format 13 Support (LBAF13)
187:184	LBA Format 14 Support (LBAF14)
191:188	LBA Format 15 Support (LBAF15)
383:192	Reserved
4095:384	Vendor Specific (VS)

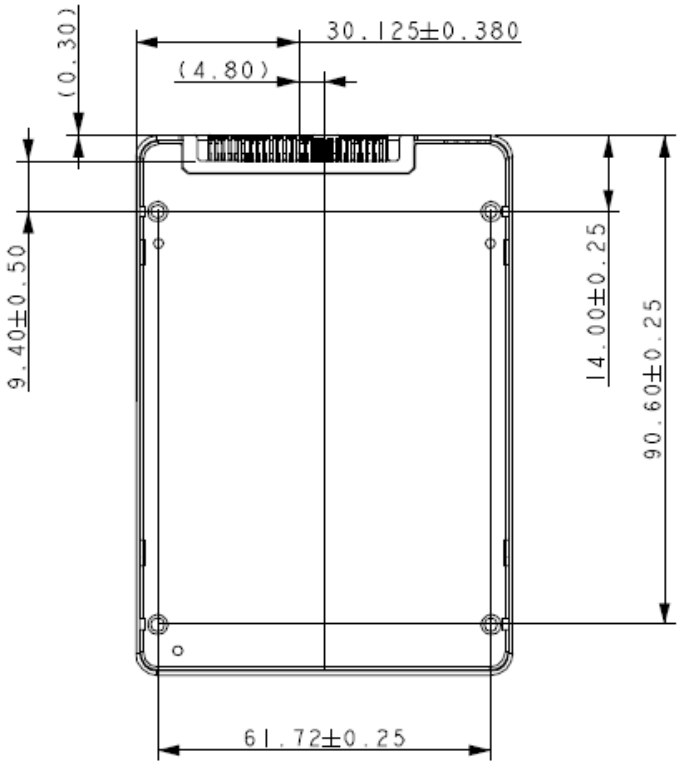
Table 6-6 List of Identify Namespace Data Structure for Each Capacity

Capacity (GB)	Byte[7:0]: Namespace Size (NSZE)
240	1BF244B0h
480	37E436B0h
960	6FC81AB0h
1920	DF8FE2B0h
256	1DCF32B0
512	3B9E12B0
1024	773BD2B0
2048	DF8FE2B0

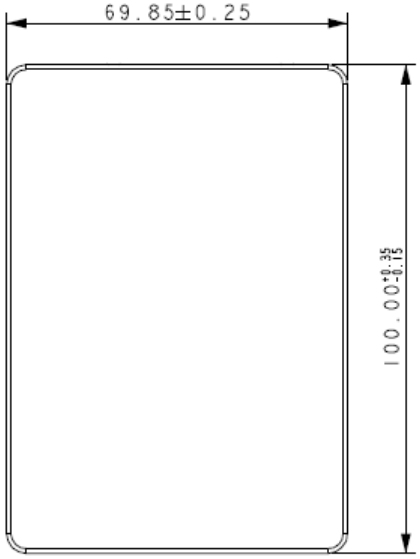
7. PHYSICAL DIMENSION

❖ 100.00mm (L) x 69.85mm (W) x 9.50mm (H)

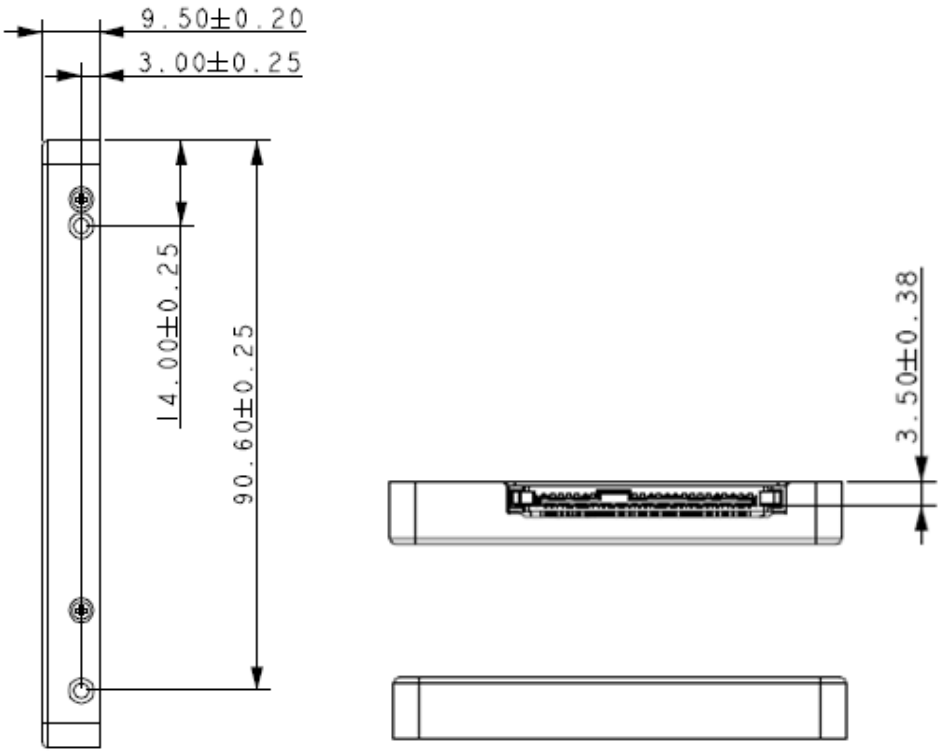
Bottom View



Top View



Side View



8. PRODUCT WARRANTY POLICY

Warranty period of the Product is twelve (12) months from the date of manufacturing. In the event the Product does not conform to the specification within the aforementioned twelve (12) -month period and such nonconformity is solely attributable to Phison's cause, Phison agrees at its discretion replace or repair the nonconforming Product. Notwithstanding the foregoing, the aforementioned warranty shall exclude the nonconformity arising from, in relation to or associated with:

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(2) failure to comply with Phison's instructions;

(3) Phison's compliance with downstream customer or user indicated instructions, technologies, designs, specifications, materials, components, parts;

(4) combination of the Product with other materials, components, parts, goods, hardware, firmware or software; or

(5) alternation, modification made by customer (including customer's suppliers or subcontractors or downstream customers) ; or

(5) other error or failure not solely attributable to Phison's cause (including without limitation, normal wear or tear, manufacturing or assembly wastage, improper operation, virus, unauthorized maintenance or repair).

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9. REFERENCE

The following table is to list out the standards that have been adopted for designing the product.

Table 9-1 List of References

Title	Acronym/Source
RoHS	Restriction of Hazardous Substances Directive; for further information, please contact us at sales@phison.com or support@phison.com.
M.2	http://www.pcisig.com
PCI Express Base 3.0	https://www.pcisig.com/specifications/pciexpress/base3/
NVM Express Specification Rev.1.2b	http://www.nvmexpress.org/
Solid-State Drive Requirements and Endurance Test Method (JESD219A)	http://www.jedec.org/standards-documents/docs/jesd219a

10. TERMINOLOGY

The following table is to list out the acronyms that have been applied throughout the document.

Table 10-1 List of Terminology

Term	Definitions
ATTO	Commercial performance benchmark application
DDR	Double data rate (SDRAM)
ASPM	Active States Power Management
APST	Autonomous Power State Transition
LBA	Logical block addressing
MB	Mega-byte
GB	Giga-byte
TB	Tera-byte
MTBF	Mean time between failures
PCIe	PCI Express / Peripheral Component Interconnect Express
S.M.A.R.T.	Self-monitoring, analysis and reporting technology
SSD	Solid state disk